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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

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First Named Inventor or Application Identifier	Katzneslon, Ron D.		
Express Mail Label No.	EK174399614US		

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

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1. [ ] Fee Transmittal Form *(Submit an original, and a duplicate for fee processing)*
2. [✔] Specification [Total Pages 8] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [✔] Drawing(s) *(35 USC 113)* [Total Sheets 8]
4. Oath or Declaration [Total Pages 16]
   a. [ ] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)* ***[Note Box 5 below]***
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. [ ] Incorporation By Reference *(useable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [✔] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] Small Entity Statement(s) [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
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NAME	Law Office of Robert C. Strawbrich				
ADDRESS	1303 Daytona Drive				
CITY	Austin	STATE	TX	ZIP CODE	78733
COUNTRY	USA	TELEPHONE	(512) 263-8169	FAX	(512) 263-8168

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RATIONAL FREQUENCY SYNTHESIZER EMPLOYING DIGITAL COMMUTATORS

Inventor(s): **Ron D. Katznelson**

Authored by: Robert C. Strawbrich
1303 Daytona Drive
Austin, TX 78733
(512) 263-8169
(512) 263-8168 (FAX)

Express Mail Information

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RATIONAL FREQUENCY SYNTHESIZER EMPLOYING DIGITAL COMMUTATORS

BACKGROUND OF THE INVENTION

It is often required to synthesize a signal source having a frequency which is a rational factor *n/m* times an existing reference or clock frequency. This need for synthesis may include cases where *n* and *m* are relatively prime and typical implementation of such synthesizers involves the use of phase locked loops ("PLL") operating on prescaled (divided) frequency versions of the desired signal and the reference or clock signal. These PLL synthesizers typically use a comparison frequency that is a small fraction of the reference or clock signal and thus produce synthesized signals on the desired frequency but with phase noise limitations due to frequency division. In such applications, the phase noise power is proportional to the square of the division ratio.

It is the object of the instant invention to provide for a synthesizer that permits rational synthesis, i.e. synthesis of a signal source having a frequency which is a rational factor *n/m* times an existing reference or clock frequency, without incurring phase noise degradations thereby providing for a signal source with phase noise essentially equal to that of the reference signal.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Figure 1 shows the first element of the preferred embodiment. A Periodic Pattern Generator **10** provides a plurality of periodic signals g_0 , g_1 through g_N where N is the number of output signals from the Periodic Pattern Generator. In the embodiment of Figure 1, a circulating shift register **12** is used to generate these signals. A "shift" signal on line **15** appears at a rate q times lower than the clock (reference) signal on line **16**. Initializing the content of Shift Register **12** is accomplished by means of the Initializer Logic Control unit **11** by loading a digital bit pattern through parallel lines **14** upon the "Load" command on line **13**. An alternative Periodic Pattern Generator may be

constructed using other means known in the art such as counters and decoders or periodic state machines having multiple taps. In an examplary embodiment of the present invention using shift register **12**, a square wave pattern is initially loaded (in this case three consecutive "1's" and three consecutive "0's") although, as will be subsequently discussed, other patterns may be advantageous for certain spectral purity requirements. For the square waveform circulating in shift register **12**, the resulting waveforms of the periodic signals g_0 , g_1 through g_N are shown in Figure 2. As can be seen, these are phase shifted versions of a square wave having a period of $N*q$ times that of the reference clock signal. We refer to the frequency associated with this period as the 'shift register frequency' or the 'periodic state machine frequency' which in this case is $f_C /(N q)$, where f_C is the reference clock frequency. The periodic signals g_0 , g_1 through g_N are fed to a Phase Commutator **20**, which is an N way digital multiplexer that is controlled by MUX control lines **22** and provides an output digital signal $f(t)$ on line **21**. The periodic operation of the Phase Commutator **20** is governed by the decoded state of counter **24**. Upon each clock cycle, decoder **23** decodes a different state of counter **24** and thus controls the commutator's slider to select a different signal g_j to be connected to the output line **21**. If every signal line from g_0 , g_1 through g_N is selected sequentially in order, the period of the Phase Commutator **20** can be as low as N times that of the reference. If one includes in the drive of counter **24** an internal pre-divider of the reference clock by an integer p, than the Commutator **20** frequency is $N*p$ times lower than that of the reference clock signal. We call this frequency the 'commutator frequency' which is given by $f_C /(N p)$. Because the periodic signal's phase available to the slider of the Commutator **20** is advancing through the sequential selection of signals g_0 , g_1 through g_N, one can regard the Phase Commutator's action as providing at its output a signal $f(t)$ with a phase which is a discrete-time step approximation to a continuous linear phase shift with time. This is shown in Figure 3 for a case in which $N = 6$. In reference to Figure 3, the phase trajectory of the signal $f(t)$ is depicted as a step trajectory **30**, having six equal phase steps per cycle of the Phase Commutator. It can be seen that it is a discrete time approximation to the linear phase trajectory **31** shown as a straight broken line.

Those skilled in the art of signal parameters would now appreciate that a signal undergoing a linear phase shift with time is simply a signal whose original frequency is translated or changed. The amount of frequency shift is simply given by the slope of the phase trajectory and is equal to the inverse of the time period over which a total phase shift of 2π takes place. In the example of Figure 3, this frequency shift is equal to the commutator's rotation frequency, which is one sixths of the clock frequency. It can be appreciated that in the above example, the phase shift steps are positive, meaning that the frequency shift is positive, resulting with a higher signal frequency. By reversing the Phase Commutator **20**'s slider rotatation direction to the opposite direction (clockwise), the phase trajectory as in Figure 3 assumes a negative slope, corresponding to a negative frequency shift. An equivalent frequency decrement effect can be achieved by keeping the Phase Commutator **20** operating in its original direction but reversing the bit shift direction for shift register **12**. In either case, the relative direction of phase shift determines whether the frequency shift (or frequency conversion) is upwards or downwards. This frequency conversion effect is equivalent to frequency mixing known in the art, and as such, the upward conversion and downward conversion is equivalent to Single Side Band (SSB) mixing with resultant Upper Side Band (USB) and Lower Side Band (LSB) mixing components respectively.

In another mode of the preferred embodiment of the instant invention, the slider of Phase Commutator **20** may be advanced by k signal lines per each clock cycle rather than one, thereby providing the output sequence g_0, g_k, g_{2k}, g_{3k} where the subscript index is valued modulo N. This is shown for example in Figure 3 by phase trajectory **32**, which now approximates a continuous linear phase shift trajectory **33**. As can be seen in this example the resultant phase slope is doubled, meaning that the conversion frequency shift is twice that related to trajectory **30**. In this case there are only three phase sampling points per cycle, which degrades the quality of the approximation of a linear phase shift trajectory. However, as long as there are more than two phase samples per cycle (Nyquist Sampling Criterion), a significant energy at the intended shifted frequency will be present within the output signal $f(t)$. However the spectral purity will be poorer than that which

results from a Phase Commutator having a larger number (N) of phase shifted signal lines.

A qualitative depiction of the amplitude spectrum of the output signal $f(t)$ as a function of frequency is shown in Figure 4. The intended frequency of the output signal is shown to posses a spectral component **40**, having a dominant energy component in comparison to all other components. The commutator frequency **40** is shown on a frequency scale that is centered about it for discussion purposes. The frequency scale uses integral units of the shift register frequency **42**. The spectral components **43, 44,45** and **46** are due to the odd harmonic content of the square wave nature of the signals g_j provided by the Periodic Pattern Generator **10**, and are related respectively to the 3rd, 5th and 7th harmonics of the square wave provided by the Periodic Pattern Generator **10**. Note that other lower level spectral components **47** may be present. It can be shown mathematically that the relative levels of spectral components **47** are related to the resolution of phase increments (to the value of N) and to the relative congruence of the commutator frequency and the shift register frequency. For commutator frequencies sufficiently high compared to that of the shift register cycle, components **47** can be made progressively small with the increasing values of N. This is due to the fact that as N increases (keeping the commutator and shift register frequencies constant), the phase trajectories **30** of Figure 3 asymptotically approach the continuous linear phase trajectory **31**. Of course, higher values of N would require faster clock frequencies for obtaining the same frequency at the output of the Phase Commutator. Moreover, it will be appreciated that the increase in N would also necessitate higher complexity in implementing the Periodic Pattern Generator **10** and the Phase Commutator **20**.

Turning back to the resultant frequency of the output signal, based on the foregoing discussion, it should be understood that the dominant desired frequency component due to the frequency conversion is shifted by an amount equal to $f_C\, k\, s\, /(\, N\, q)$ with a sign dependent on the rotation direction of the commutator and where we designate the rotation direction by the sideband value s assuming values of +1 or –1. By cascading

several commutators of order N driven for different rotation rates, one can obtain a signal with resultant frequency R_O given by

(1) $R_O = f_C\,[(k_1 s_1)/q_1 + (k_2 s_2)/q_2 + \ldots]/N$

This is due to the cascaded mixing nature of the commutators. Thus, signals whose frequencies constitute a rich set of possible rational values for R_O / f_O can be generated with these structures – imparting the term Rational Synthesizer to the embodiments as described.

The Phase Commutator shown in Figure 1 has only one output. In order to provide for cascading of commutators and in order to obtain best spectral purity results, it would be advantageous to have a commutator with multiple sliders that commutate sequentially over the input signals g_0 , g_1 through g_N and consequently provide a sequence of output signals f_0 , f_1 through f_N all having similar spectral characteristics but with different phases. In that way, cascading that well preserves the phase sampling integrity can be made possible. An example of a rational synthesizer using cascaded commutators is shown in Figure 5. In this example, Commutator Cell 2 has three inputs ($N = 3$) and three outputs. It is cascading Commutator Cell 1, which is a subsampled $N = 6$ commutator running on its own independent counter. In figure 6, a cascade of two independent four way commutators ($N = 4$) is shown. There is considerable advantage in using four way commutators since they provide a good compromise of phase sampling resolution and implementation complexity while maintaining appreciable frequency of operation. This is because of very efficient designs available for four way digital multiplexers. Detailed description of embodiments and applications using the four way commutator-based rational synthesizers of the present invention are provided in a copending application entitled "Rational Frequency Synthesizers" filed on May 25, 2000 for the benefit of a common assignee, which is incorporated herein by this reference in its entirety. According to the present invention, an example of a full four-way commutator with four inputs I1, I2, I3 and I4 and having four outputs O1, O2, O3 and O4, is shown in

Figure 7. The decoder (not shown) commands the operation of the commutator via control lines C1 through C4 in order to effect the proper sequential routing of the commutator.

Generally, for an N way rational synthesizer commutator we designate the m^{th} output signal from a commutator as a function of time by $f_m(t)$ and we note that it is periodic and thus can be represented by its Fourier spectral components which we designate as $F_m(n)$. Here, n is the harmonic index of the frequency which is n times the fundamental period. The input signals to the commutator as functions of time are designated as $g_0(t)$, $g_1(t)$ through $g_N(t)$. If these signals have more generally, not one cycle within the N stage shift register, but r complete cycles, it can be shown that the Fourier spectrum of the output signals is given by

$$(2) \qquad F_m(n) = \frac{rNq}{2\pi(r+sq)} \exp[2\pi i s m n/(qN)] \sum_{l=-\infty}^{l=\infty} \left[\frac{G(l)\exp[-2\pi i s m r l/(qN)]}{rl-n} \right] H(l)$$

where $H(l)$ is an indicator function of l given by

$$(3) \qquad H(l) = \begin{cases} 1 & \text{whener } l(sr+q) - sn = qNu \text{ ; were } u \text{ is an integer} \\ 0 & \text{otherwise} \end{cases}$$

and where $G(l)$ is the Fourier coefficient at frequency l of the periodic signal $g_0(t)$.

By inspecting Equation (3) one notes that nonzero Fourier coefficients will only be at frequencies n for which the linear Diaphontine equation in integers l and u at the top part of the definition of $H(l)$, has solutions. Using number theoretic tools one finds that for a square wave form of $g_0(t)$ (and hence, only odd order harmonics l) the offset frequencies n for which there is nonzero power is given by

(4) $n = \mu d + sq + r$; where d is the greatest common denominator of $2(sr+q)$ and qN

It is therefore possible to choose the parameters such that d is maximized, providing maximum spectral purity clearance about the desired frequency $sq+r$.

Figure 8. shows an embodiment of the rational synthesizer with a PLL using six way commutator with a non-square wave pattern, designed specifically to offer better second order spectral purity. It also incorporates a differential DSB mixer for applications requiring high frequency mixing and further incorporates a differential phase detector PD which permits the propagation of the symmetry into the differential low pass filter.

What is claimed is:

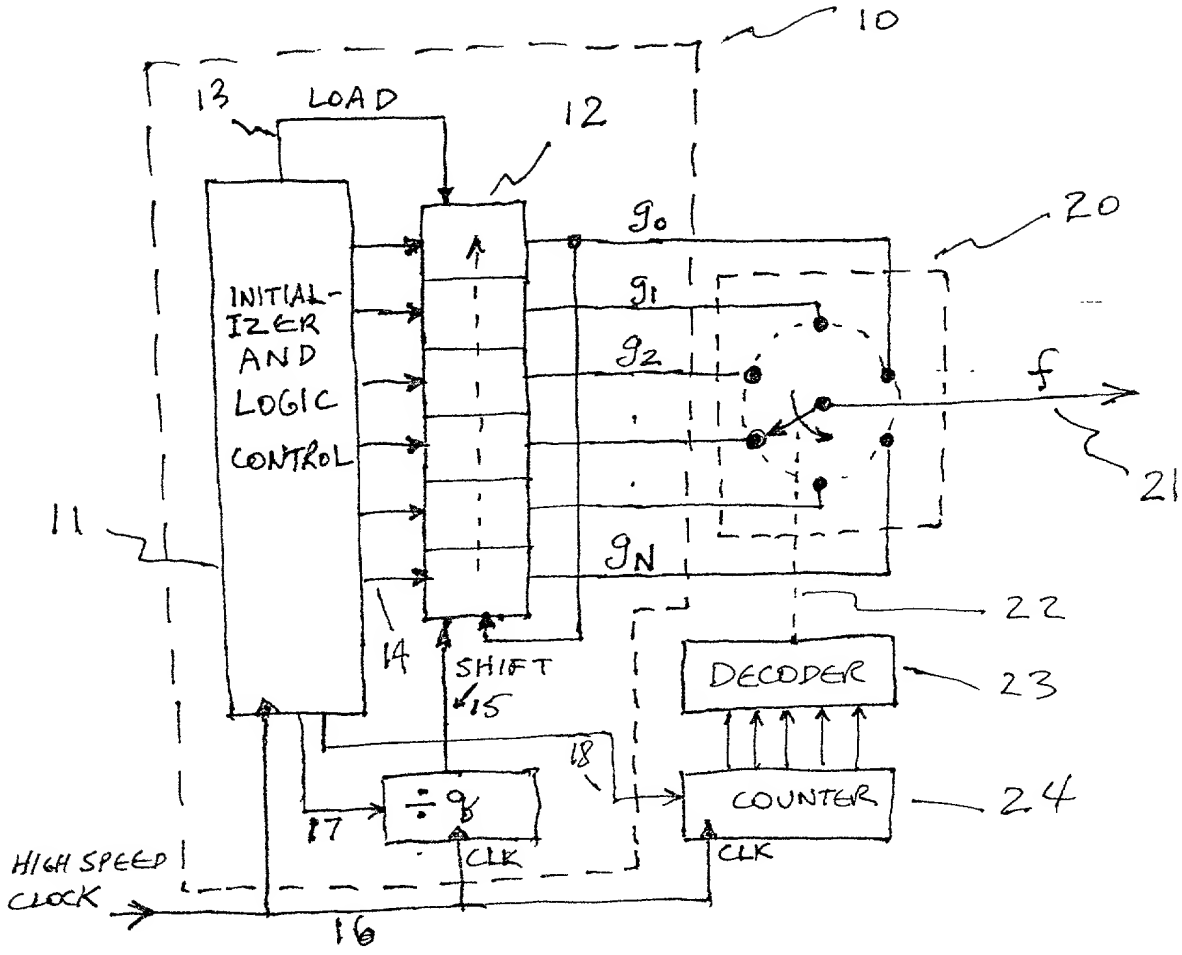
1. A method for rational digital synthesis comprising the steps of

providing a periodic pattern signals

feeding said periodic pattern signals to an N way commutator

clocking the periodic pattern generator at a frequency f1; and

crotating the commutator at a frequency f2, therby obtaining an output frequency of f1+/- f2.


10
13
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12
20
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g_1
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11
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SHIFT
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DECODER
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24
CLK
CLK
HIGH SPEED
CLOCK
16

FIGURE 1

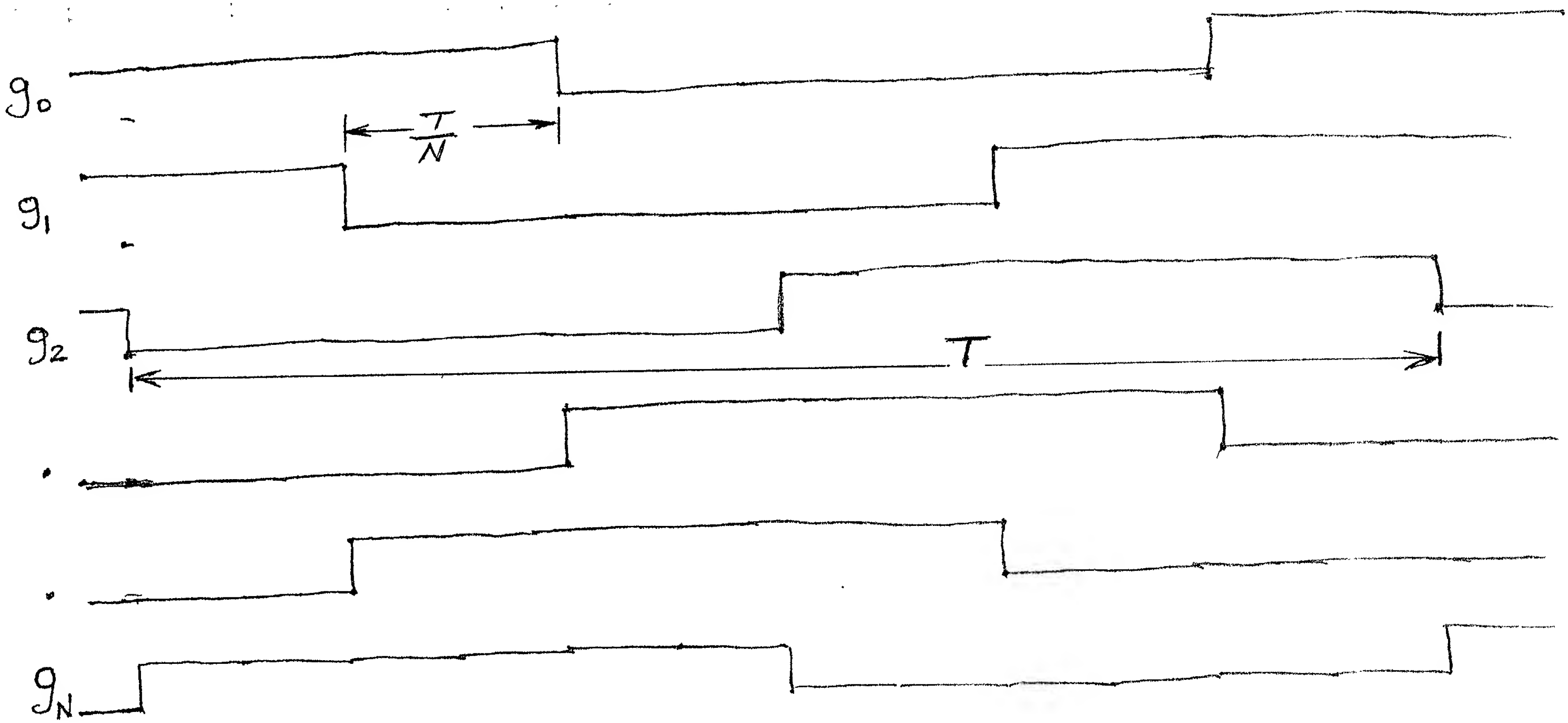


FIGURE 2

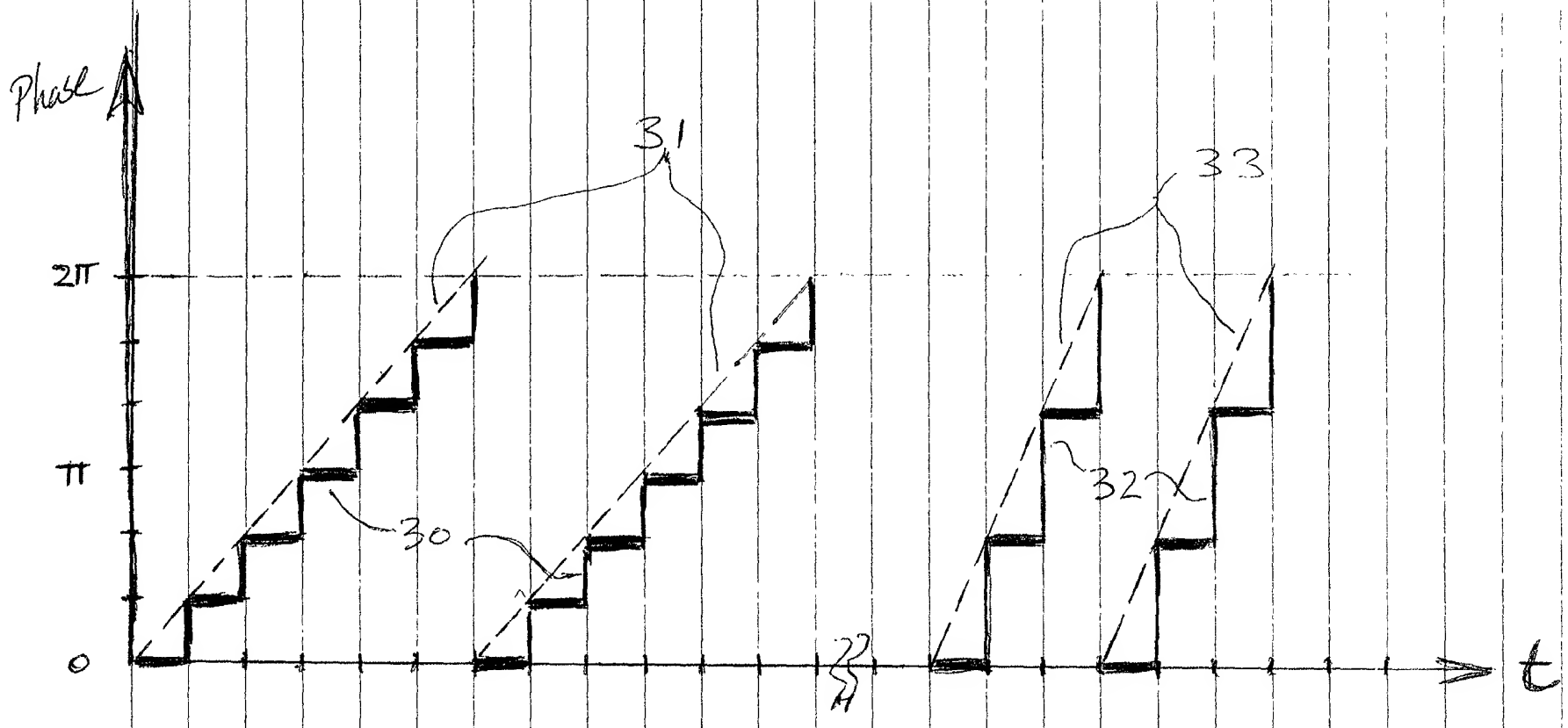


FIGURE 3

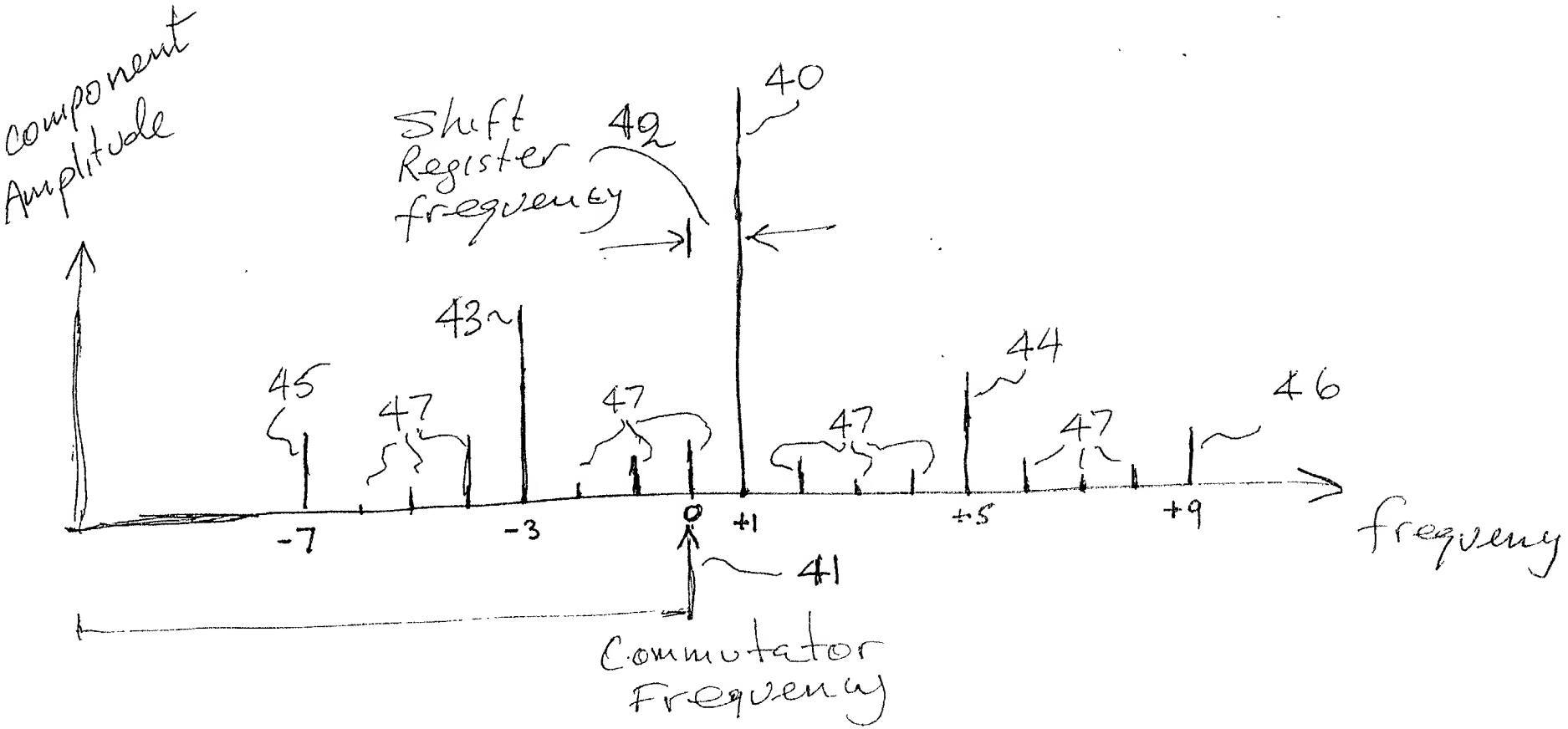
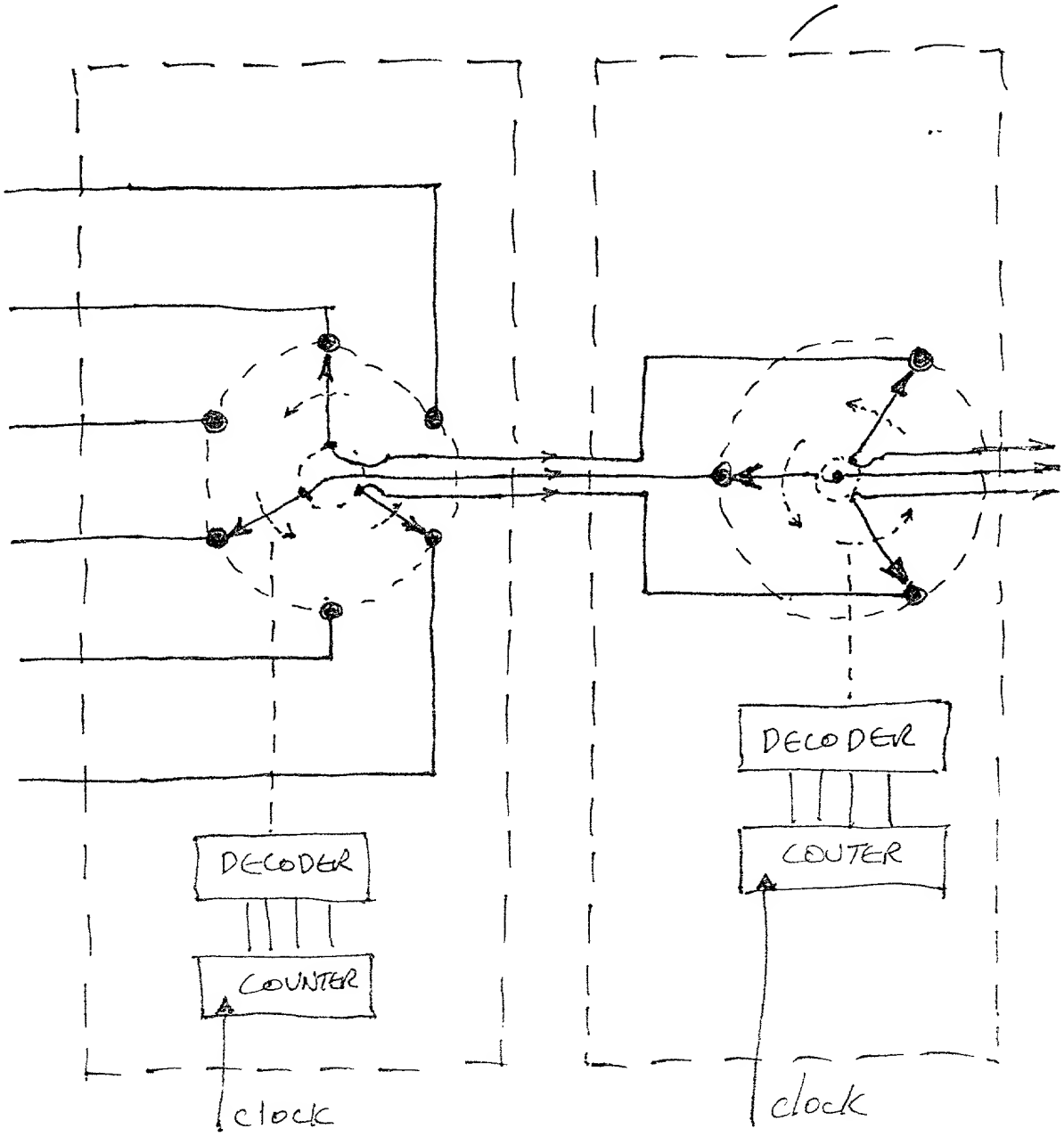


FIGURE 4



COMMUTATOR CELL 1

COMMUTATOR CELL 2

FIGURE 5

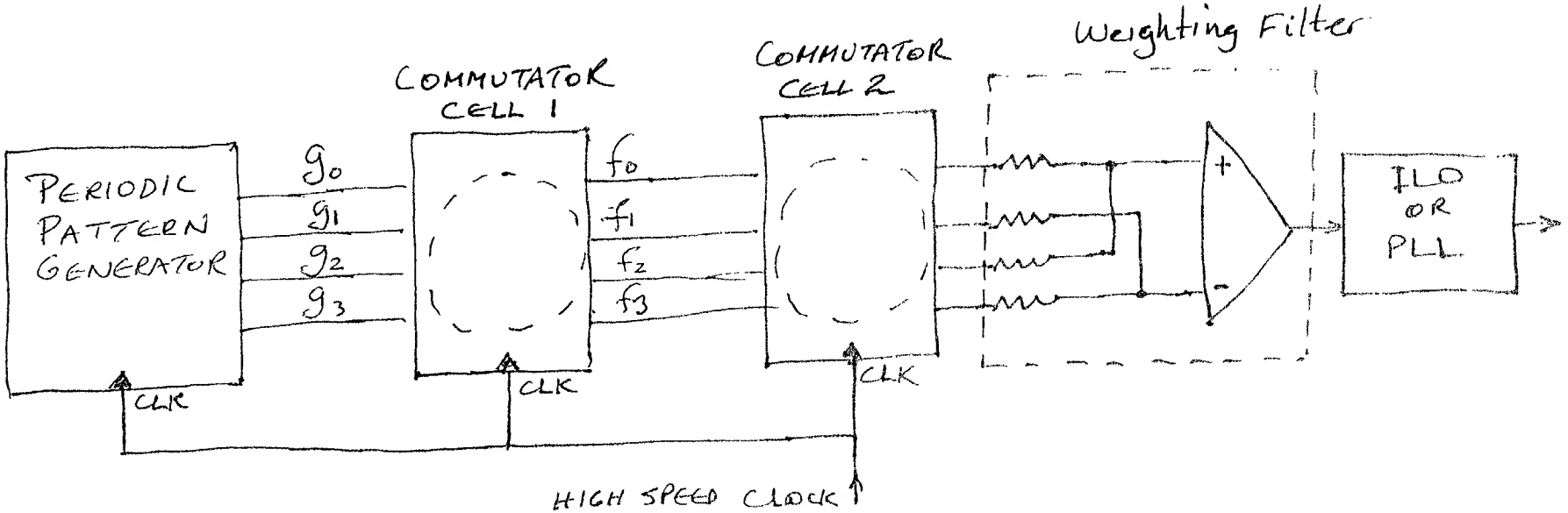


FIGURE 6

Figure 7

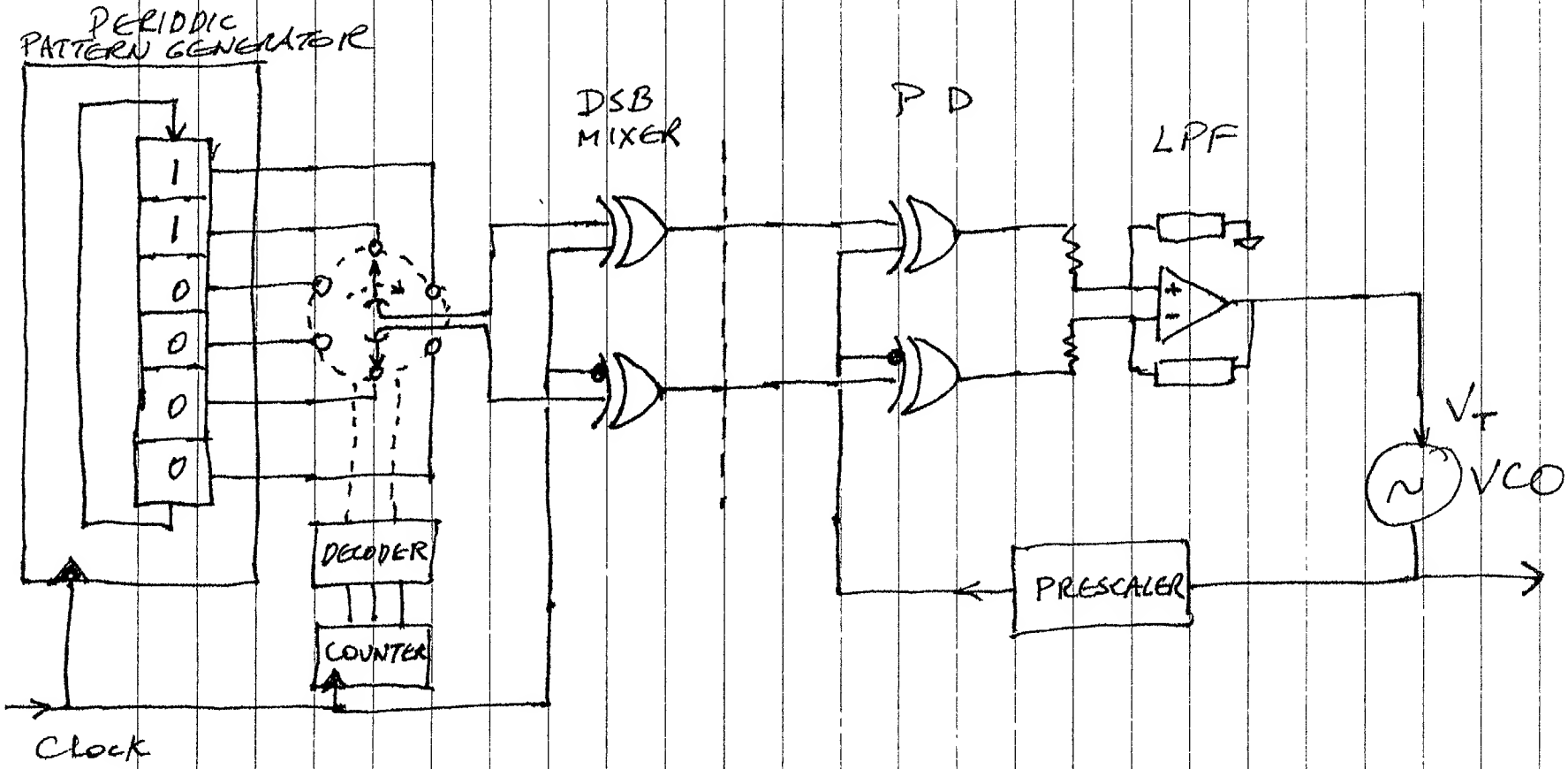


FIGURE 8